Chip Scale Package Implementation Issues

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ABSTRACT

Availability of board solder joint reliability information is critical to the wider implementation of Chip Scale Packages (CSPs). The JPL-led CSP Consortia (Ref. 1) of enterprises representing government agencies and private companies have jointed together to pool in-kind resources for developing the quality and reliability of CSPs for a variety of projects. In the process of building the Consortia test vehicles, many challenges were identified regarding various aspects of technology implementation. This paper will present our experience in the areas of technology implementation challenges, including design and building both standard and microvia boards, and assembly of two types of CSP test vehicles.

CSP implementation Challenges

Emerging grid Chip Scale Packages (CSPs), miniature version of ball grid arrays (BGAs), are competing with bare die flip chip assemblies. Figure 1 Shows miniaturization trend from quad flat packages (QFF) to BGA and CSP. CSP is an important miniature electronic package technology for utilizing especially low pin counts, without the attendant handling and processing problems of low peripheral leaded packages such as thin small outline packages (TSOPs) and high I/O (input/output) QFPs. Advantages include self alignment characterization during assembly reflow process and better lead (ball) rigidity. Reliability data and inspection techniques are needed for CSPs acceptance especially for high reliability applications.

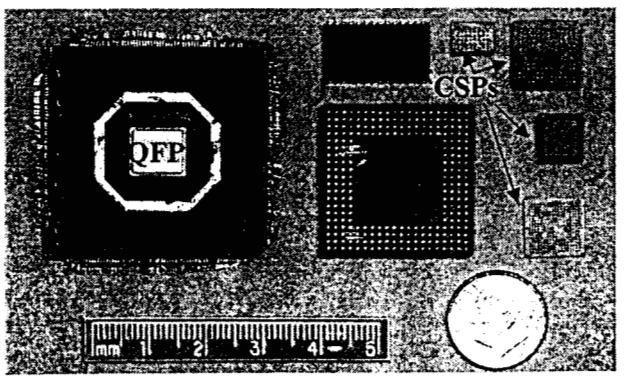

Figure 1 Miniaturization trend from QFP to BGA and CSP

Two concepts of CSPs are shown in Figure 2. The concepts presented include: (1) packages with flex or rigid interposer and (2) wafer level molding and assembly redistribution.

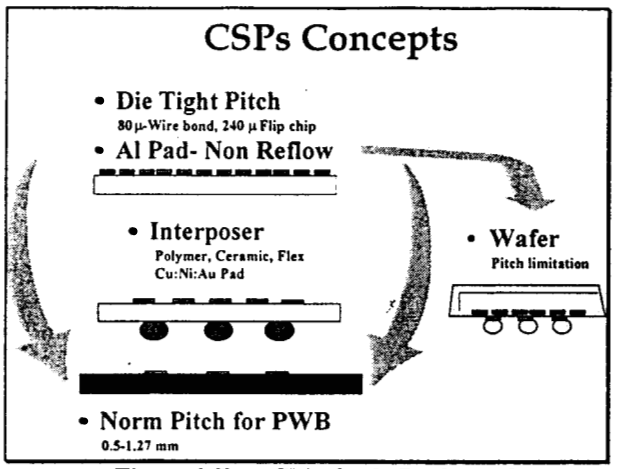

Figure 2 Two Chip Scale Package Concepts

Figure 3 compares advantages and disadvantages of CSP to bare die assembly. Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.
- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPs do not permit significant redistribution and the current cost effective PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation.
- Eases die functionality testing and improve reliability.

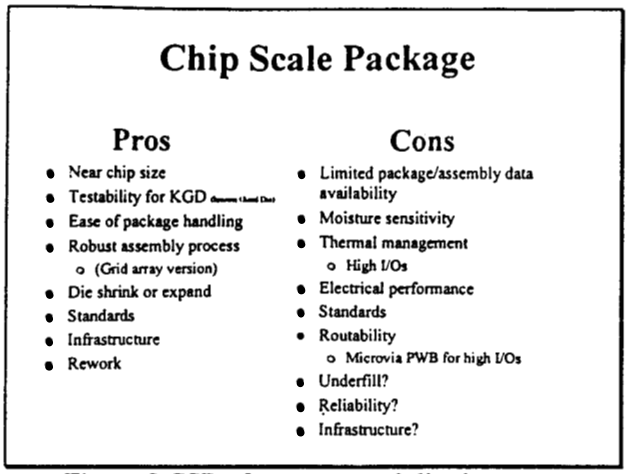

Figure 3 CSP advantages and disadvantages

Ease of Manufacturing Gid CSPs

CSPs can be categorized into grid arrays and leads (or no leads) using the I/O expandability and manufacturing robustness as shown in Figure 4.

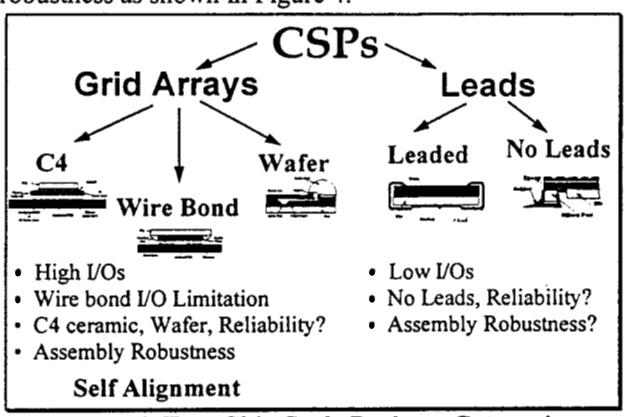

Figure 4 Two Chip Scale Package Categories

Key advantages/disadvantages of each category are also listed. The mini (fine pitch) grid arrays can accommodate higher pin counts, and similarly to BGAs, they have self alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published (See Ref. 2) as one of their attributes. This attribute has permitted reduction in the number of solder joint defects to lower levels than conventional SM leaded packages.

For grid CSPs, the molten surface tensions are much smaller than BGAs since they have lower solder ball volumes. This, coupled with the CSPs finer pitch, can degrade their self alignment performance, especially with heavy packages. Therefore, the CSPs might require much tighter placement accuracy than the 50 mil pitch BGAs.

CSP Implementation Challenges

In the process of building the NASA-JPL-industry CSP consortium test vehicles many challenges were identified regarding various aspects of technology implementation. Key challenges are summarized as follows:

Industry and "Expert" Definition of CSP

Although the expression of CSP is widely used by industry from suppliers to users, its industry definition had evolved as the technology has matured. At the start of the package's introduction into market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package.

A rapid transition to a much lower size was difficult both by package suppliers and end user. Suppliers had difficulty in building packages with such a definition whereas the users had difficulties with accommodating the need for the new microvia printed circuit board (PWB) because of routing requirement and its increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using standard PWB design rather than the microvia build to avoid cost.

The "expert definition" undermines one of the key purpose of the package allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

Therefore, in reality, CSPs are miniature new packages that industry is starting to implement and there are many unresolved technical issues associated with their implementation. Technical issues themselves also changes as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. New issues included the use of flip chip die rather than wire bond in CSP. Flip chip failure within the package is a potential new failure mechanism that need to be considered.

Package Availability in Early 1997

CSP's availability in daisy chain for the attachment reliability characterization was one of the challenging issues at the start of the program in early 1997. There were numerous publications on a wide range of CSPs, but most packages were in early development and lacked

package reliability information. Assembly reliability data were even rarer. Most packages were only available in prototype form, and this, of course, did not guarantee the package similarity to the production version or even their future availability.

More than a six month delay in package delivery date was the norm. Four packages dropped from the program, and one was delayed almost a year with last moment modification by supplier. Although many suppliers promoted their packages and package reliability, they were not willing to submit their packages for an independent evaluation, possibly because of lack of confidence.

Numerous packages from leaded and leadless to grid CSPs were chosen for evaluation. At the start of program, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O, 0.5mm package, was dropped by the manufacturer prior to the trial test vehicle assembly. Therefore, the maximum I/O package become a CSP with 275 I/Os. Three other higher I/O with 0.5mm pitch were also dropped prior to full build. A hard metric, 0.5mm, CSP package with 188 I/O with data given by supplier for the English pitch version, was among these three packages. The supplier was unable to meet our last build schedule, late in 1998.

These trends clearly indicate that the package suppliers were struggling to build CSPs with 0.5mm, especially with high I/O counts.

The majority of the next phase of the CSP program have pitches of 0.8mm. In this phase, there are a few high I/O CSPs with 0.5mm pitch. This indicates that industry is starting to be more comfortable with moving towards a tighter pitch at higher I/O.

Lack of Design Guidelines

Guidelines and standards on various elements of CSPs were not available. For example, there was missing package daisy chain information, and insufficient mechanical drawing data to begin with. The majority of packages were hard metric, however, a few with the inch pitches caused dimensional errors because of decimal round off when converted from inch to metric. Furthermore, ball and pad information needed for board design was missing and it was time consuming to gather information from suppliers since most needed to be generated by technical personnel.

There was no information on pad design relative to package pad for achieving optimum reliability. Pads for PWBs could be assumed to be the same as package, as a rule of thumb. For our design, guidelines developed by the package suppliers were used when available. Otherwise, available knowledge and engineering judgment were utilized.

Need for Microvia PWB

The standard PWB design could be used for low I/O CSPs. Build up (microvia) board technology is required for higher I/O CSPs in product with active die. For daisy chain packages, it is possible to design high I/O on a standard board. Board design guidelines are needed, especially for the build up (microvia) configuration.

I/O Limitation

There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM (surface mount) packages, direct chip attachment (DCA), BGAs, and CSPs on one board is another expected design and assembly challenge. This mixed technology was designed and its implementation issues are being studied.

CSP Reliability Challenges

CSP reliability data and inspection techniques are needed for its acceptance especially for high reliability applications.

Reliability, irrespective of its definition, is no longer an "after-the-fact" concept; rather, it must be an integral part of development and implementation. This is specifically true for microelectronics with demands for miniaturization and system integration in a faster, better, and cheaper environment. CSPs rapid development and introduction into the market is a good example of this trend.

The use of new materials, processes, and new applications obscure the traditional definition of quality and reliability assurance. New systems approaches are needed to assure quality and reliability as well as to manage risks. Quality should be assured by design for reliability, controls for processes, tailored testing methods for qualification, and use of unique accelerated environmental testing along with credible analytical prediction. In other words, an efficient concurrent engineering system approach must be implemented.

Environmental Testing

Among the many environmental accelerated testing methodologies for assessing reliability of electronic systems, thermal cycling is the most commonly used for characterization of devices as well as interconnections. Among the many predefined thermal cycling profiles, the military and commercial aspects represent the two

extremes. Previously, NASA also had a preset specific thermal cycling requirement. The Military Standard 883 (Mil-STD-883) has widely used for the benchmark testing. Within Mil-STD-883, there are three levels of accelerated cycling temperatures:
Condition A, -55°/85°C
Condition B, -55°/125°C
Condition C, -65°/150°C

For benchmark conditions, devices are generally subjected to condition C and assemblies most often to condition B. The assemblies were traditionally considered qualified when they last 1,000 cycles. A commercial cycling profile, the J-12 IPC specification, recommends a thermal cycle in the range of 0°C to 100°C. Within a temperature range, the dwell, heat and cool down rates are critical parameters and also affect cycles to failure.

The NASA thermal cycling requirements are stringent and are specified in various revisions of NASA Handbooks. For example, in a previous revision, NHB 5300.4 (3A-1), there was a well defined requirement for number of cycles and solder condition after exposure. No cracking of any solder joint was allowed after 200 NASA cycles (-55°C to 100°C with 245 minutes duration).

Performance-based Assurance Requirement

In a subsequent NHB revision, the requirements were based on meeting the specific mission condition. The build and test methodology is expected to yield confidence in reliability to satisfy the mission conditions. Mission requirements are emphasized rather than a universal cycle and a value for all missions.

Test to "establish the confidence in reliability" adopted by NASA a long-time ago is now "the reliability theme" for the commercial sector. Discussions on "Breaking Traditional Paradigms" and "Rethinking of Environmental Reliability Testing" by authors from the commercial sector are becoming hot topics with the introduction of new miniaturized CSPs. These packages have their own unique form factor not seen in SMT. Unable to meet the stringent requirements established by the previous military standards, a new "paradigm shift" is considered to be the solution. The "shift" is further motivated by several factors including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology
- Obsolescence of many military specifications

Additional unique tests are now adopted to meet the specific consumer electronic products. For portable electronics, bend test, drop test, and possible "washing machine test" are suggested. The IPC 9701 specification, Qualification and Performance Test Methods for Surface Mount Solder Attachments, is aimed to include some of these requirements. It must be recognized that no accelerated tests can be truly universal. Field reliability is the ultimate test, and either substantiates or invalidates the experimental tests.

For space missions, gathering information on the root cause field failure is almost impossible. For commercial applications, rapid changes in technology render field information almost useless for new product development. The only solution is to understand key reliability parameters and to design for reliability. Subsequent process controls, as well as efficient qualification and inspection, also help assure sufficient field reliability. In other words, risk control and risk management must be practiced.

ASSEMBLY AND RELIABILITY

The Consortium has assembled about 200 test vehicles which considered numerous variables including board design, standard and microvia, single and double sided, different surface finishes, and different board materials.

Manufacturing of grid package indicates that they are robust. For example, no defects were observed when thirty test vehicles, each with 4 grid CSPs with 46 I/Os, were assembled.

Quality of Solder Joints

Figure 5 shows a SEM photomicrograph of a solder joint for a TAB CSP and a low I/O wafer level (8 I/O) package on a board. Low package height made inspection of the joints very difficult, either by visual or by SEM. Three of these wafer packages showed poor quality solder joints with signs of cracking. Poor quality of the package was the reason for existence of microcracks after assembly. For this reason, this package was excluded for the subsequent test vehicle assembly.

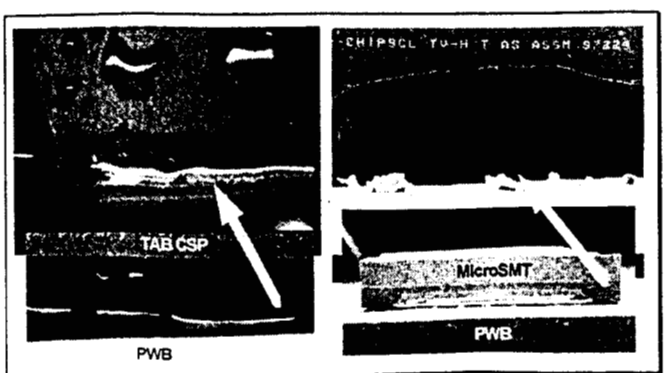

Figure 5 Good Solder Joint Quality of a Grid CSP and Poor Solder Joint Quality of Low I/O Wafer Level

CONCLUSIONS

- Mixed technology assembly may not easily permit the use of optimum solder volume to achieve the highest reliability. This is probably true for an SM mixture of fine pitch and leadless packages and become challenging with the addition of no-lead (leadless) and grid CSPs. CSPs, reliability may be degraded in a mixed technology assembly, especially for no-lead CSPs.
- A low lead small wafer level CSP packages exhibited poor quality.
- Traditionally, solder joint failure was considered to be the weakest link in the microelectronics attachment reliability. This might not be true for CSPs with innovative designs.
- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is the key to collecting meaningful test results.

REFERENCES

1. Ghaffarian, R, et al. "CSP Consortia Activities: Program Objectives and Status," Surface Mount International Proceedings, August 23-27, 1998, pp. 203-230
2. Ghaffarian, R. "Ball Grid Array Packaging Guidelines," distributed by Interconnect Technology Research Institute (ITRI), August 1998, http://www.ITRI.org

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Biography

Dr. Reza Ghaffarian has 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering. At JPL, Quality Assurance Section, he supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored nearly 100 technical papers and numerous patentable innovations. He is a frequent speaker and chaired technical conferences including SMTA International, IMAPS, ASME, SAMPE, NEPCON, and IPC. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 in engineering from University of California at Los Angeles (UCLA).